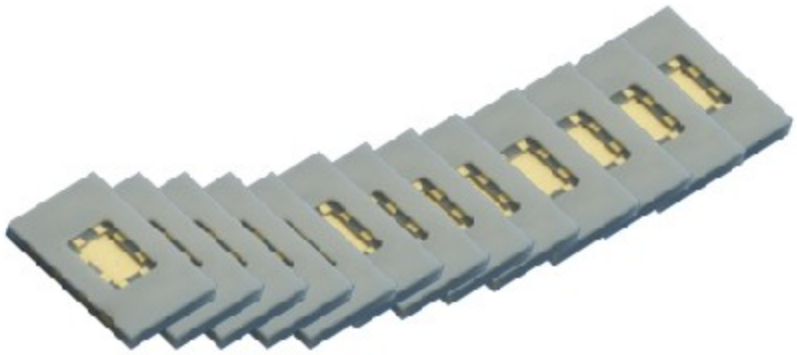
2013 Aeronautics Sensor Working Group (ASWG)
Webex
2:00 PM January 31, 2013

Packaging Technologies for 500°C SiC Electronics and Sensors

Liang-Yu Chen

Ohio Aerospace Institute/NASA GRC, Cleveland, OH 44135



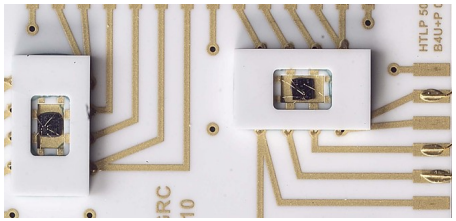
Outline

Background

- 500°C SiC electronics and sensors
- Packaging needs and packaging concept/functions

Review of ceramic substrates and thick-film metallization based packaging technologies for 500°C SiC devices

- Packaging systems for 500°C SiC electronics



- Packaging system for SiC capacitive pressure sensors

Summary

Acknowledgements

Packaging Technologies for 500°C SiC Electronics and Sensors

Background

500°C SiC electronics and MEMS sensors have been demonstrated

- JFETs and JFETs based circuits developed at NASA GRC
- MEMS based pressure sensors and Schottky diode based gas chemical sensors developed at NASA GRC
- Applications include aerospace engine control and long term Venus probes

Packaging technologies needed for long-term test and eventual commercialization of 500°C SiC electronics and sensors

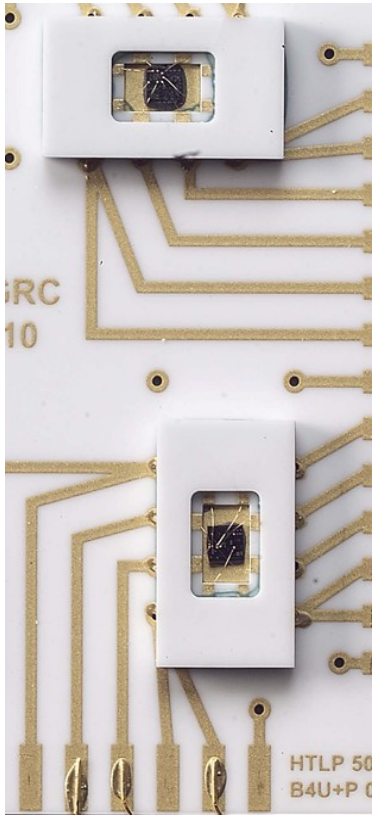
Conventional packaging materials fail/degrade at high temperatures

- Plastic materials melt, de-polymerize, and burn at 500°C
- Alloys (solder) melt and oxidize rapidly at 500°C
- High thermal stress due to thermal expansion mismatch can cause permanent mechanical failure at structure level

Background: Packaging Concept

Packaging Technology for Electronics/Sensors

- Packaging is essential to microelectronics and sensors
  - Mechanical support
  - Electrical interconnection
  - Electromagnetic, chemical environment
- Chip-level packaging
  - Substrate and metallization
  - Die-attach
  - Wire-bonding
- Printed Circuit Board (PCB)
  - Interconnecting packaged chips and passives
- PCB edge connectors
  - Subsystem level packaging
- Capacitive pressure sensor packaging
  - Spark-plug type
  - High differential pressure environment



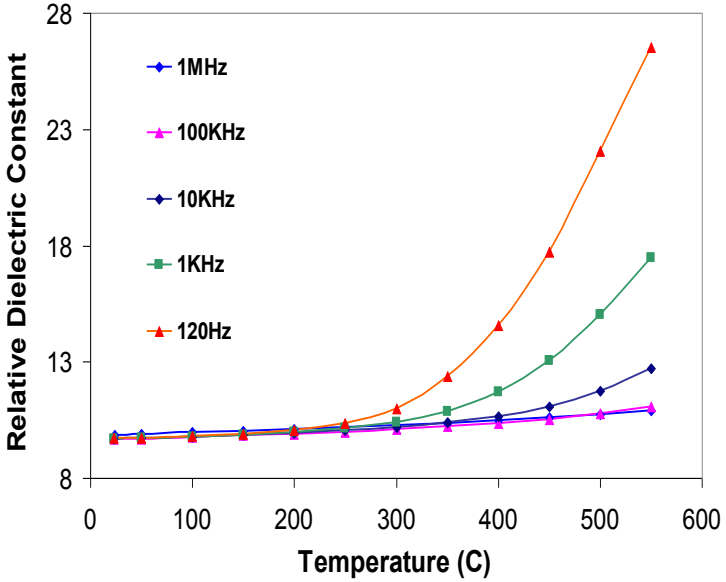
Packaging Systems for 500°C SiC Electronics

Performance of Ceramic Substrate Materials

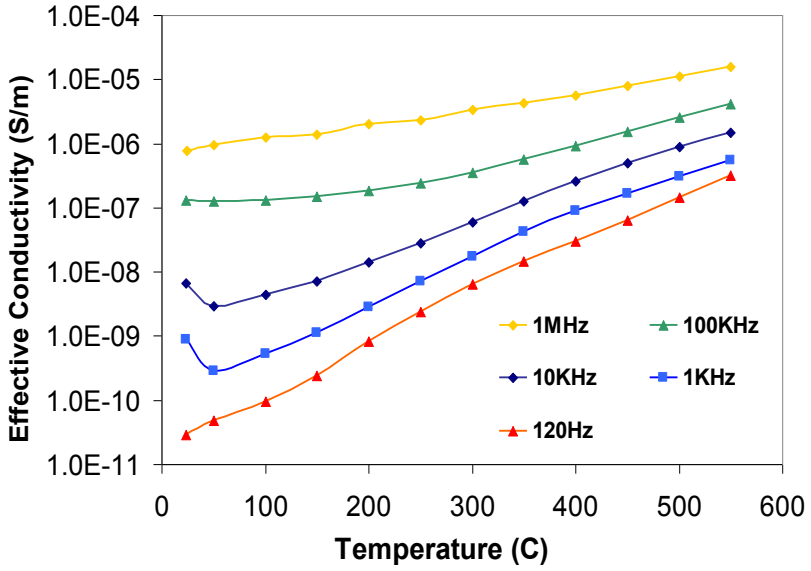
Required dielectric properties of substrate materials at high temperature

- Stable and low dielectric constant at elevated temperatures
- Low dielectric loss at elevated temperatures

Dielectric Constant of 96% Al_2O_3



AC Conductivity of 96% Al_2O_3

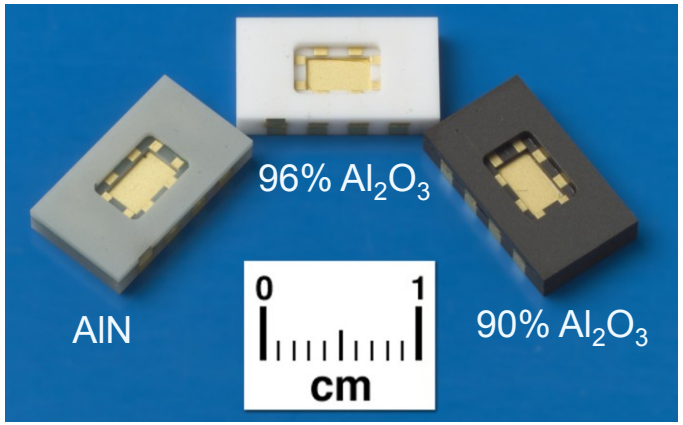


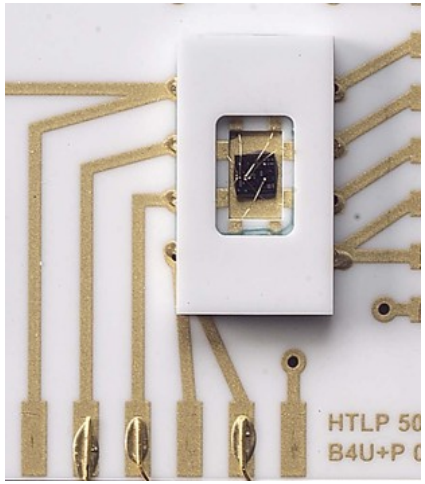
- The challenge for 500°C packaging technologies is at the materials level
- Compared with other ceramic substrate materials tested, 96% alumina has better dielectric performance at high temperatures

Chen and Hunter, 2004 MRS

Packaging Systems for 500°C SiC Electronics

Ceramic Chip-level Packages and PCBs

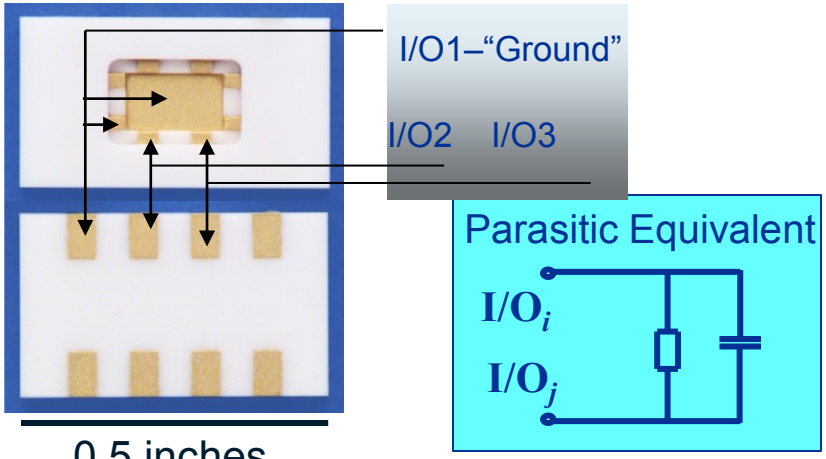


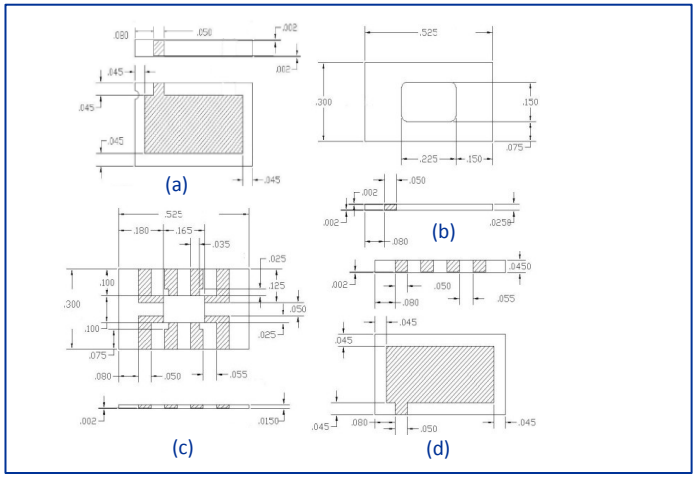


- Three types of ceramics and Au thick-film metallization based chip-level packages and printed circuit boards (PCBs)
- Chip-level packages characterized between room temperature and 500°C
- An edge connector in development for PCB – PCB (subsystem-level) interconnection

Packaging Systems for 500°C SiC Electronics

96% Alumina Chip-level Packages





Chen and Hunter, 2005 HiTEN

Parasitic Capacitance and Conductance of Neighboring I/Os

T (ºC) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	< 5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	0.5	0.5	0.5	1	1	1	1.5	1.5	1.5	1.5	2
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.0005	0.001	0.001
1K	0.5	0.5	0.5	0.5	0.5	0.5	0.6	0.7	0.7	0.8	0.95
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.001	0.002	0.0025
10K	0.49	0.50	0.50	0.490	0.49	0.52	0.53	0.58	0.59	0.65	0.69
	0.001	0.000	0.000	0.000	0.000	0.001	0.002	0.003	0.004	0.006	0.008
100K	0.492	0.486	0.497	0.493	0.487	0.517	0.539	0.535	0.563	0.585	0.57
	0.005	0.006	0.0015	0.002	0.003	0.005	0.007	0.011	0.015	0.022	0.030
1M	0.501	0.497	0.485	0.506	0.499	0.529	0.533	0.55	0.556	0.544	0.55
	-	-	-	-	-	-	-	-	-	-	-

Usable for packaging many envisioned low power 500°C devices/ circuits

> 50°C margin above 500°C

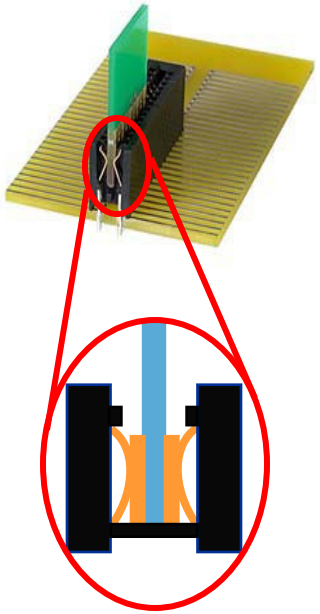
pF

µS

Packaging Systems for 500°C SiC Electronics

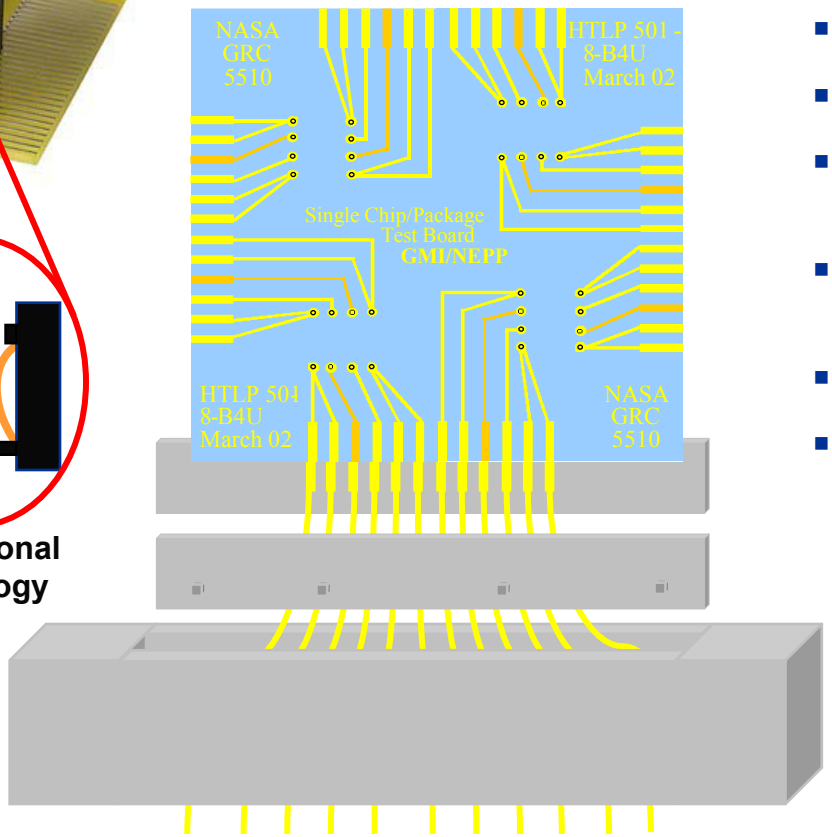
PCB Edge Connector for 500°C Low Power Electronics

- Subsystem Level Interconnection



Conventional Technology

High temperature edge-connector

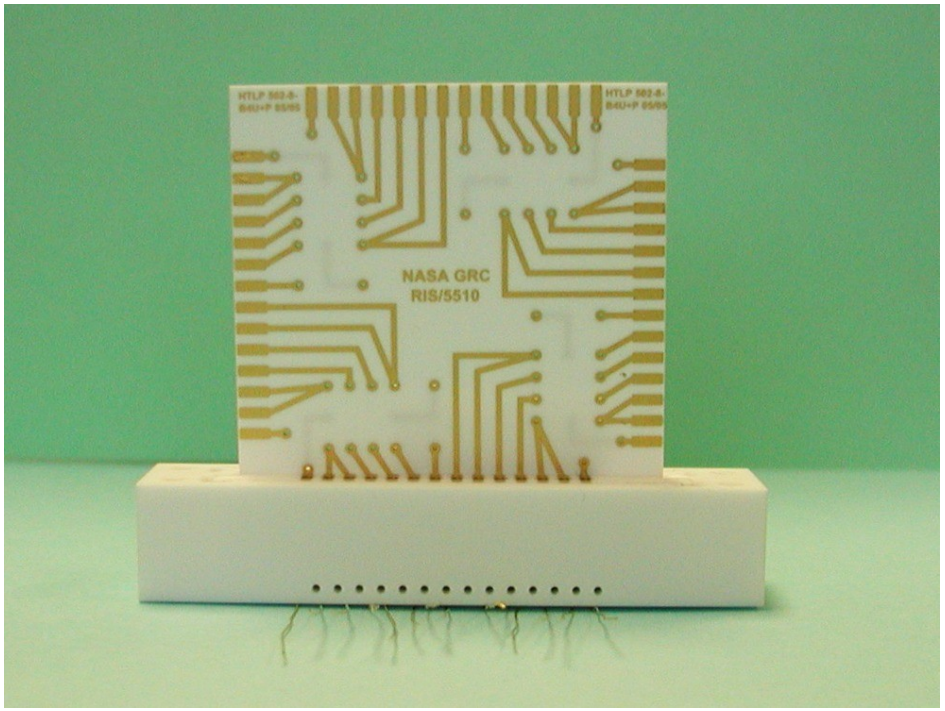


- 500°C operation
- Ceramic structure
- Compatible metallization with PCBs
- 15 mil wires with fiber insulation sleeves
- High temperature alloy contacts
- Challenges
  - Fabrication of ceramic parts
  - Diffusion at high temperatures
  - Plastic deformation of spring materials

Packaging Systems for 500°C SiC Electronics

PCB Edge Connector for 500°C Low Power Electronics

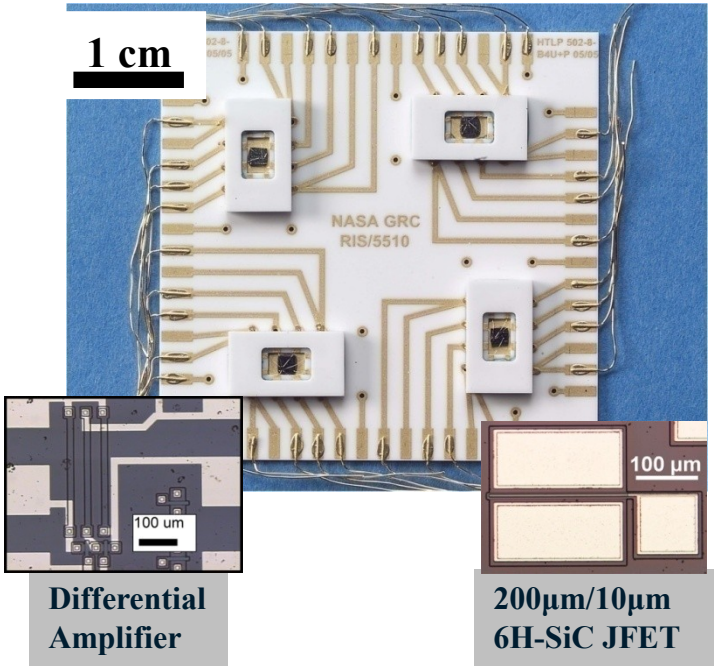
- Subsystem Level Interconnection

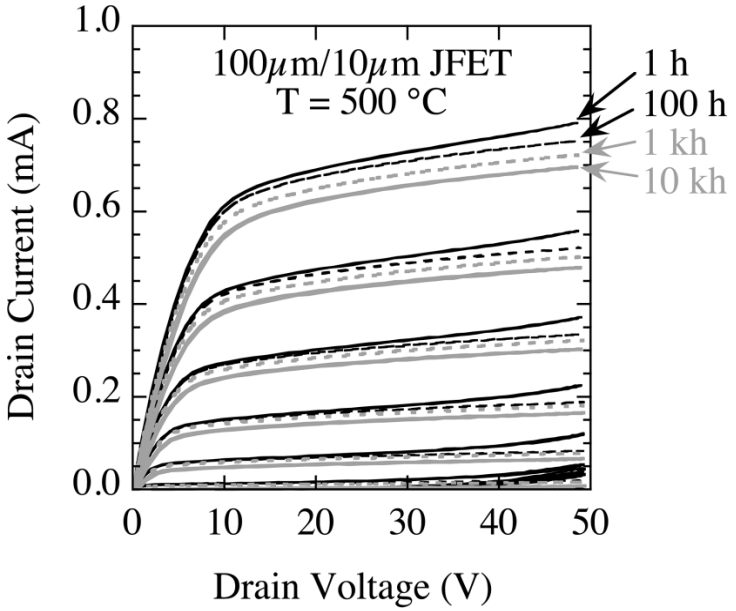


- PCB level interconnection
- For 500°C operation
- 96% alumina structure
- High temperature thick-film metallization
- 10 mil Au wires with fiber insulation sleeves
- High temperature alloy springs for electrical contacts
- Tested at 500°C, further improvement underway

Packaging Systems for 500°C SiC Electronics

Test Results of Packaged SiC JFET



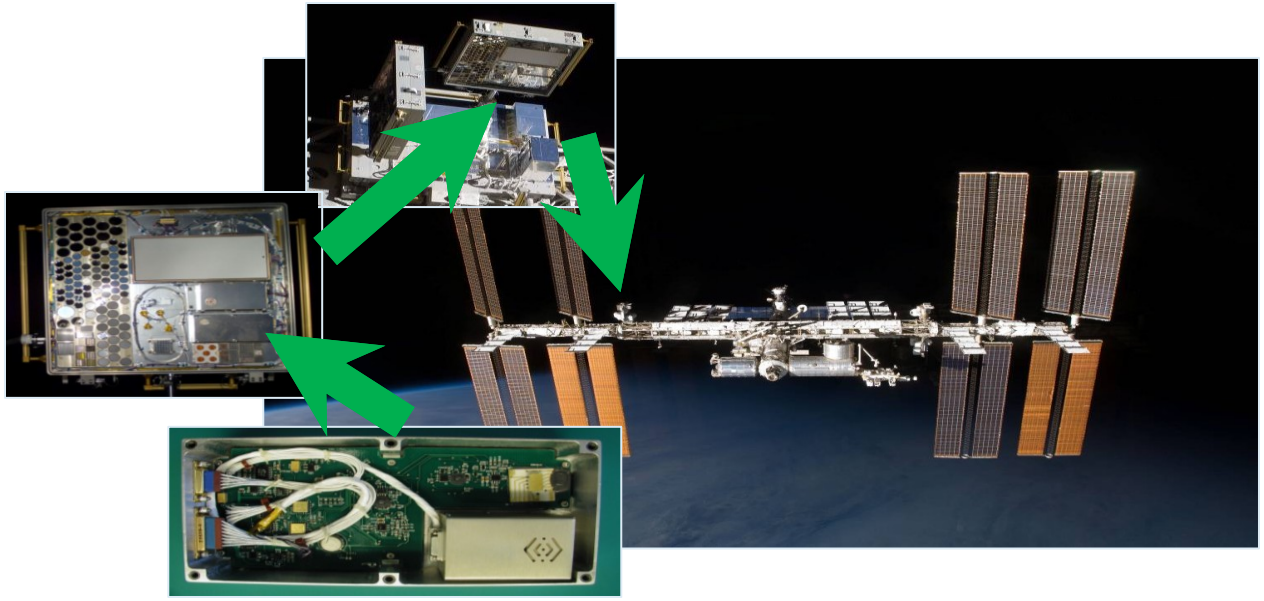


Neudeck, Spry, *et al*, 2008 ECSCRM

- Packaged SiC JFETs and JFETs based IC characterized at 500°C
- 96% alumina packaging system
- less than 7% change in the JFET characteristics in first 6000 hours
- Tested at 500°C for over 10,000 hrs
- Demonstrated for long term operation at 500°C for the first time
- Thermal cycling tested between room temperature and 500°C

Packaging Systems for 500°C SiC Electronics

Space and Flight Test of 96% Alumina Packaging System



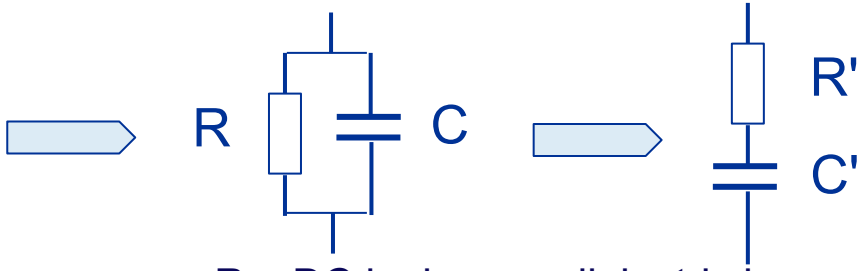
- MISSE7 suite exposed to Shuttle launch, atomic oxygen, space radiation, thermal cycling, and reentry
- The data acquiring circuit board in an aluminum box
- I-V curves of packaged SiC JFETs recorded every hour for eighteen months on ISS orbit
- No failure/degradation detected

Prokop et al, 2010 National Space & Missile Materials Symposium

Packaging Systems for 500°C SiC Electronics

- Improvement of AlN packages with Dielectric Glass Coating

Dielectric layer



$$\begin{cases} R' = R(\omega,T)/[1+\omega^2 R^2(\omega,T)C^2(\omega,T)] \\ C' = \dfrac{1+\omega^2 R^2(\omega,T)C^2(\omega,T)}{\omega^2 R^2(\omega,T)C(\omega,T)} \end{cases}$$

R – DC leakage + dielectric loss

C – Electrical polarization effect

$$Z(\omega,T) = R'(\omega,T) + \frac{1}{j\omega}\frac{1}{C'(\omega,T)}$$

Two-layer dielectric systems

$$Z(\omega,T) = R_1'(\omega,T) + R_2'(\omega,T) + \frac{1}{j\omega}\left[\frac{1}{C_1'(\omega,T)} + \frac{1}{C_2'(\omega,T)}\right]$$

$$\begin{cases} R_1' = R_1(\omega,T)/[1+\omega^2 R_1^{\,2}(\omega,T)C_1^{\,2}(\omega,T)] \\ R_2' = R_2(\omega,T)/[1+\omega^2 R_2^{\,2}(\omega,T)C_2^{\,2}(\omega,T)] \end{cases} \quad \begin{cases} C_1' = \dfrac{1+\omega^2 R_1^{\,2}(\omega,T)C_1^{\,2}(\omega,T)}{\omega^2 R_1^{\,2}(\omega,T)C_1(\omega,T)} \\ C_2' = \dfrac{1+\omega^2 R_2^{\,2}(\omega,T)C_2^{\,2}(\omega,T)}{\omega^2 R_2^{\,2}(\omega,T)C_2(\omega,T)} \end{cases}$$

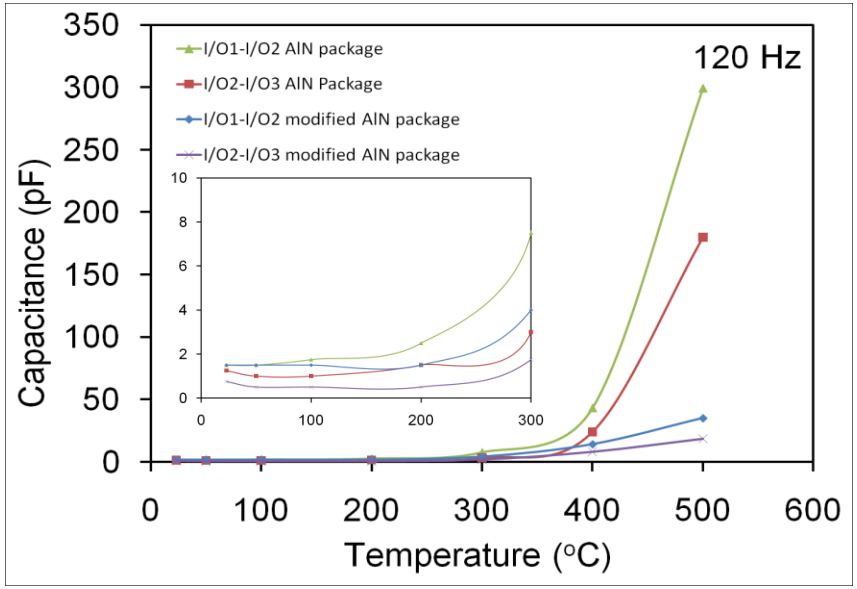
- When R_2 is very small or C_2 is very big, the impedance of layer 1 more dominant
- AlN: At 500°C, AlN dielectric constant very high at f ~100Hz, dielectric loss very high at f ~MHz
- A dielectric glass with low and stable dielectric constant and dielectric loss may reduce the capacitance at low ω, increase resistance at high ω
- The impact of glass layer at room temperature may be minimal

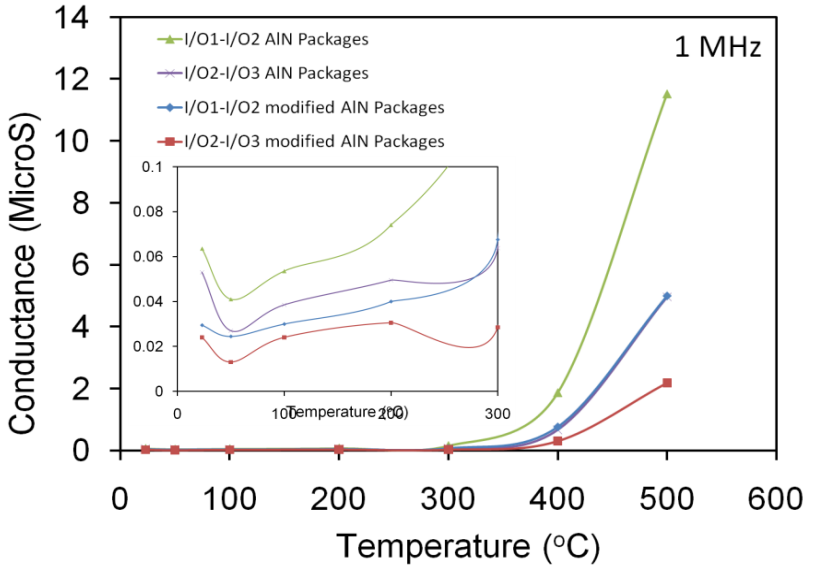
Chen, 2011 HiTEN

Packaging Systems for 500°C SiC Electronics

- Improvement of AlN packages with Dielectric Glass Coating

Improvement of AlN Chip-level Packages by Glass Coating



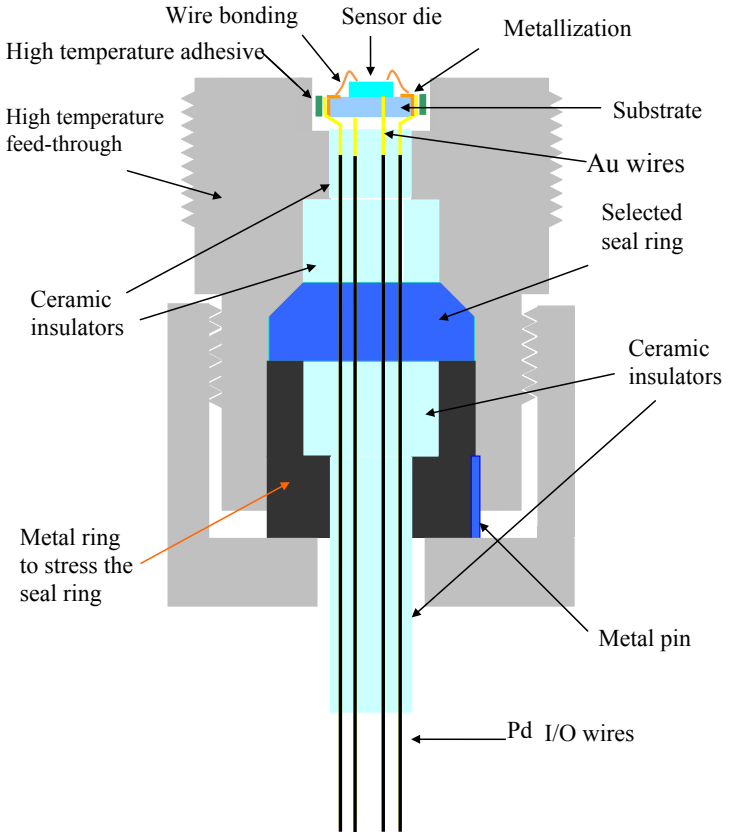


- AlN has low CTE (4.5 ppm/K) which is close to CTE of SiC (4.0 ppm/K) – better thermo-mechanical reliability
- Dielectric constant and dielectric loss of some of commercial AlN materials are very high at high temperature
- A glass coating is used to reduce parasitic parameters of an 8 I/Os low power chip-level AlN package
- Both dielectric performance and thermal stability are improved significantly

Packaging system for SiC capacitive pressure sensors

Spark - Plug Type Package for High Temperature Capacitive Pressure Sensors

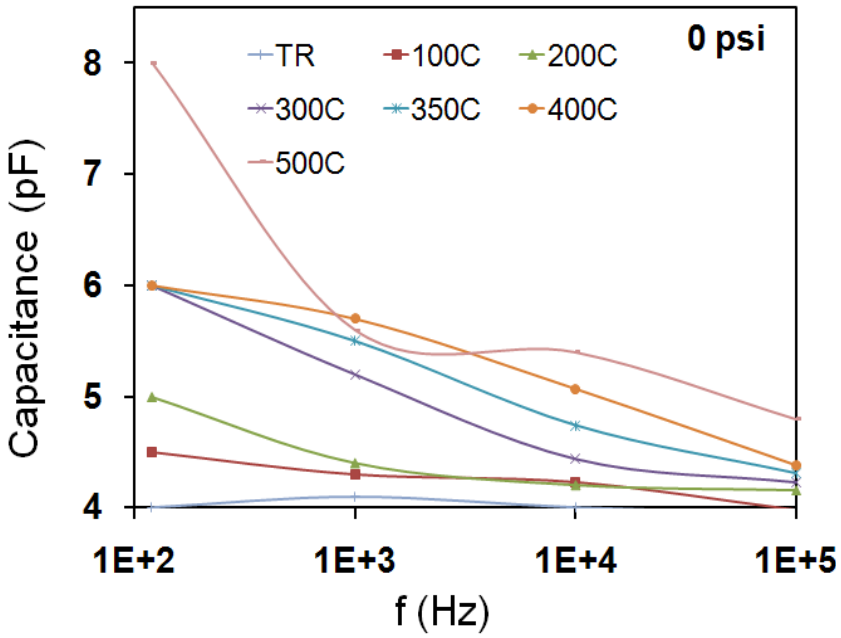
- 96% alumina substrate with Au thick-film metallization
- Four 10 mil diameter Au wires (I/Os) attached
- Au wires extended by four Pd wires
- Pd wires sealed in a commercial SS high temperature gland
- The gland operable up to 8000 psi
- Electrically characterized between RT and 500°C
- Low parasitic effects
- May apply to other micro-fabricated solid sensors

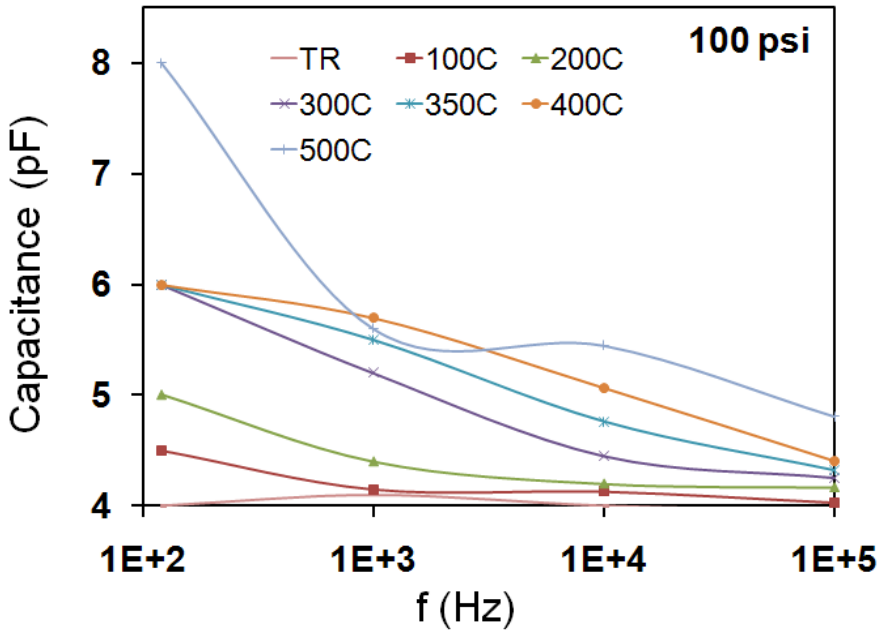


Chen, Beheim, and Meredith, 2010 HiTEC

Packaging system for SiC capacitive pressure sensors

Spark - Plug Type Package for High Temperature Capacitive Pressure Sensors

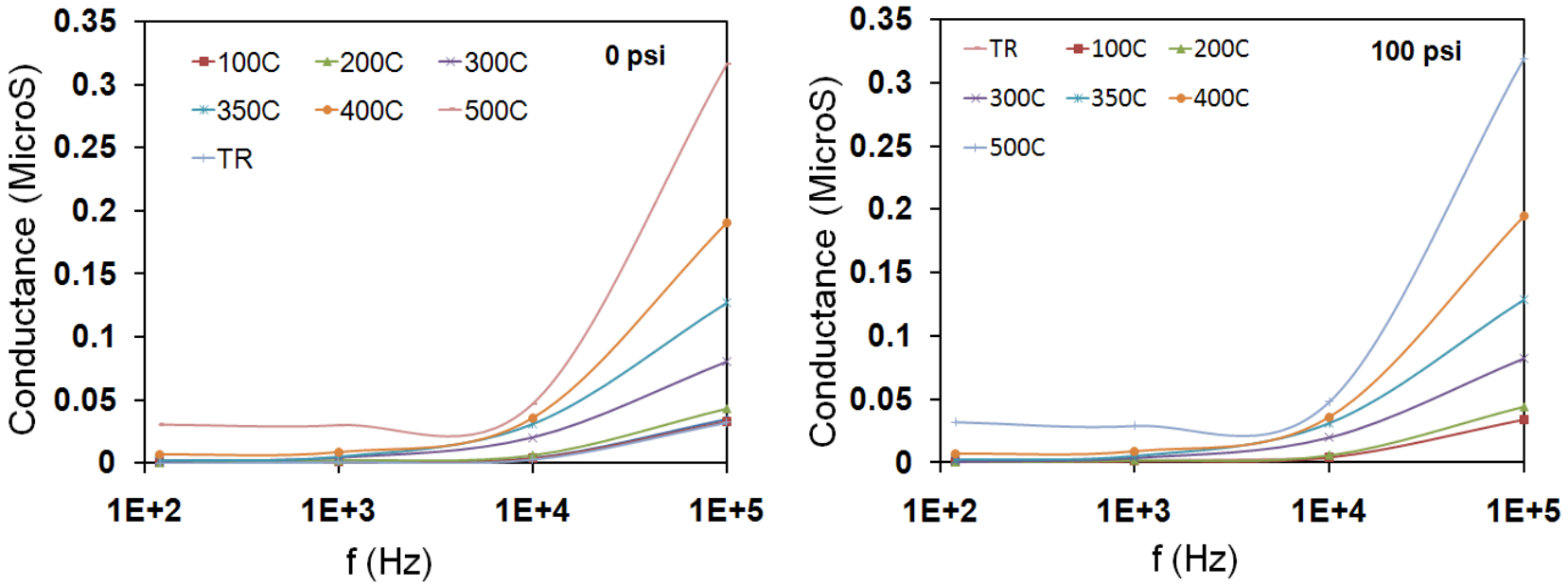




- Four-wire configuration, two wires connected to the substrate but not sensor chip, characterized as packaging parasitic parameters
- Low parasitic capacitance
- Parasitic capacitance not sensitive to pressure

Packaging system for SiC capacitive pressure sensors

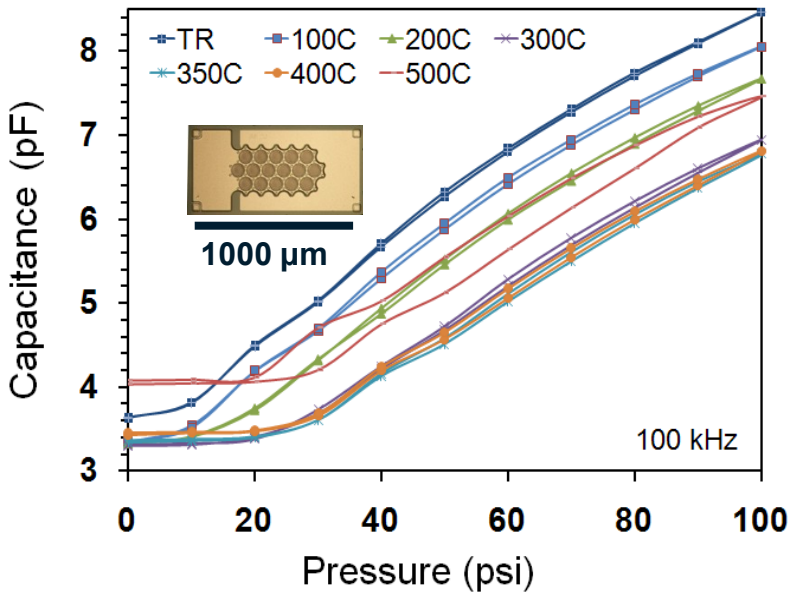
Spark - Plug Type Package for High Temperature Capacitive Pressure Sensors

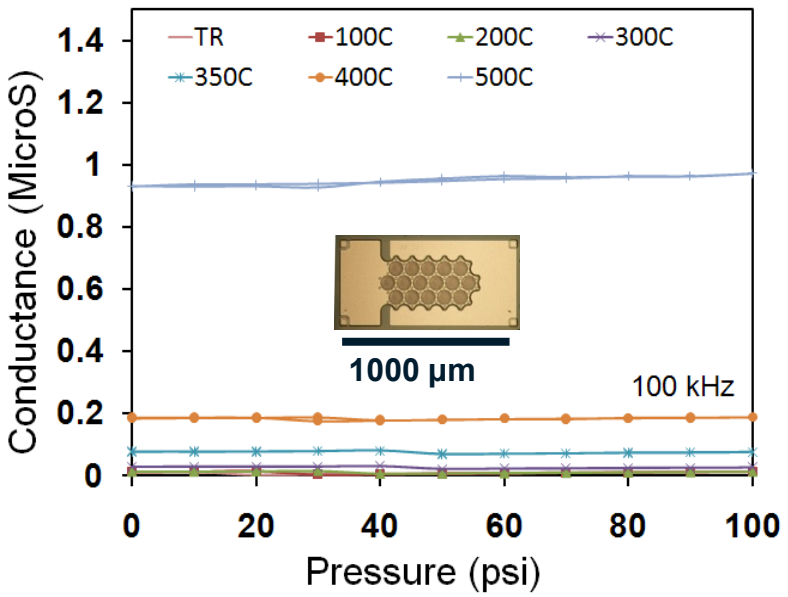


- Four wire configuration, two wires connected to the substrate but not sensor chip, characterized as packaging parasitic parameters
- Dielectric loss increases with T and f
- Dielectric loss not pressure sensitive

Packaging system for SiC capacitive pressure sensors

Spark - Plug Type Package for High Temperature Capacitive Pressure Sensors

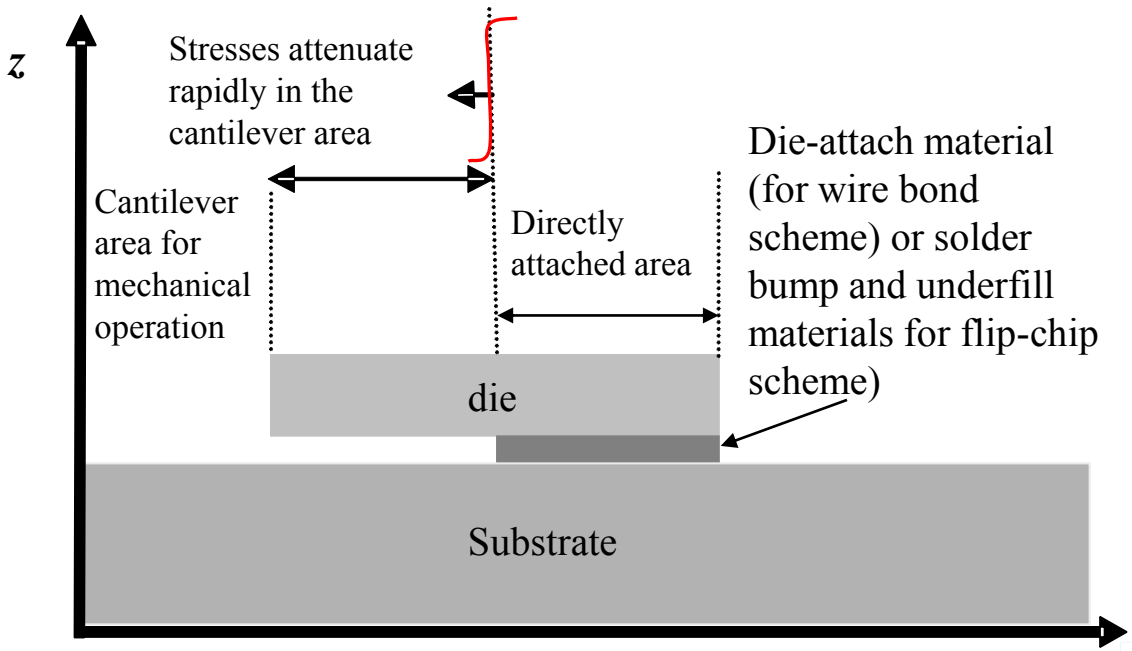




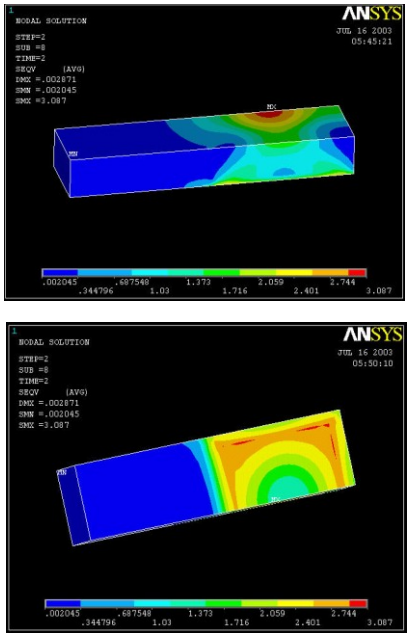
- Packaging effects subtracted
- Capacitance responds to pressure monotonically between T_R and 500°C
- Temperature calibration needed for real measurement

Packaging system for SiC capacitive pressure sensors

Low Stress Die-attach Structure for MEMS Packaging



Side view of lateral stress attenuation



Von Mises Stress contour plot of top and bottom of die

Cantilever area for mechanical operation, cantilever area is almost stress free

FEA simulation: the research group lead by Prof. McCluskey at University of Maryland

Packaging Technologies for 500°C SiC Electronics and Sensors

2:00PM January 31, 2013

Summary

Ceramic substrates and thick-film metallization based packaging systems demonstrated at 500°C

- Alumina and aluminum nitride chip-level packages and PCBs
- A compatible 96% alumina edge-connector demonstrated
- Packaged SiC JFET circuits successfully tested for over 10,000 hours at 500°C
- Packaged SiC JFET successfully tested on LEO for 18 months

A spark-plug type sensor package for 500°C sensors

- Low parasitic effects
- Characterized and tested with SiC sensors at temperatures up to 500°
- A low stress die-attach structure developed for high temperature MEMS
- This sensor package applies to high temperature and high differential pressure environments

Packaging for high temperature gas chemical sensors in process

Further development needed for higher density, higher power, higher frequency, and higher temperature applications

Thank You Very Much for Your Attention!

Acknowledgements

Author acknowledges contributions of Gary W. Hunter, Philip G. Neudeck, Glenn M. Beheim, David J. Spry, and Roger D. Meredith at NASA Glenn Research Center. Author thanks Drs. Lawrence G. Matus, Mary V. Zeller, and Gary T. Seng for proof-reading the presentation. The high temperature packaging research associated with this presentation is currently supported by Vehicle Systems Safety Technologies (VSST) project of NASA Aviation Safety program.